REMARKS

This paper is responsive to a Non-Final Office action dated April 5, 2006. Claims 1-46 were examined. Claims 1-19 were previously elected in response to the Examiner's Restriction Requirement. Claims 3–9 and 13-15 are objected to for including informalities. Claims 1-15 and 18-19 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U. S. Patent No. 6,463,570 B1 to Dunn et al. Claims 16 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dunn in view of U. S. Patent No. 5,943,488 to Raza.

Claim Objections

Claims 3 – 9 and 13-15 are objected to for including informalities.

Claim 3 is amended to clarify the claim language.

Regarding claim 4, the Office action states that it is not clear what is meant by "minimum dimension." Applicant respectfully points the Examiner to paragraph [1022] of the specification, which states:

> Referring back to FIG. 1, capacitive load 108 is generally designed to represent particular process layers and/or design rules. For example, in FIG. 3A, metal trace 302 has a line width 306 and metal trace 304 has a line width 308. These line widths may be set to the critical dimension of the metal layer (i.e., a minimum line width), a nominal line width (i.e., an average line width), or to a maximum line width that may be formed in the particular metal layer and achievable in a particular process technology. Similarly, the thickness of the metal layers including metal traces 302 and 304 and the dielectric layer(s) separating the metal layers may be varied with achievable values in a particular process technology.

Applicant respectfully maintains that claim 4 satisfies the requirements of 35 U.S.C. § 112. Accordingly, Applicant respectfully requests the objection to claim 4 be withdrawn.

Regarding claim 5, the Office action states that it is not clear what is meant by "maximum dimension." Applicant respectfully points the Examiner to paragraph [1022] of the specification, which states:

> Referring back to FIG. 1, capacitive load 108 is generally designed to represent particular process layers and/or design rules. For example, in FIG. 3A, metal trace 302 has a line width 306 and metal trace 304 has a line width 308. These line widths may be set to the critical dimension of the metal layer (i.e., a minimum line width), a nominal line width (i.e., an average line width), or to a maximum line width that may be formed in the particular metal layer and achievable in a particular process technology. Similarly, the thickness of the metal layers including metal traces 302 and 304 and the dielectric layer(s) separating the metal layers may be varied with achievable values in a particular process technology.

Applicant respectfully maintains that claim 5 satisfies the requirements of 35 U.S.C. § 112. Accordingly, Applicant respectfully requests the objection to claim 5 be withdrawn.

Regarding claim 6, the Office action states that it is not clear what is meant by "nominal dimension." Applicant respectfully points the Examiner to paragraph [1022] of the specification, which states:

> Referring back to FIG. 1, capacitive load 108 is generally designed to represent particular process layers and/or design rules. For example, in FIG. 3A, metal trace 302 has a line width 306 and metal trace 304 has a line width 308. These line widths may be set to the critical dimension of the metal layer (i.e., a minimum line width), a nominal line width (i.e., an average line width), or to a maximum line width that may be formed in the particular metal layer and achievable in a particular process technology. Similarly, the thickness of the metal layers including metal traces 302 and 304 and the dielectric layer(s) separating the metal layers may be varied with achievable values in a particular process technology.

Applicant respectfully maintains that claim 6 satisfies the requirements of 35 U.S.C. § 112. Accordingly, Applicant respectfully requests the objection to claim 6 be withdrawn.

Regarding claim 7, the Office action states that it is not clear what is meant by "minimum density." Applicant respectfully points the Examiner to paragraph [1022] of the specification, which states:

> In addition, the density, i.e., the spacing relationship between a metal trace and adjacent metal traces, as illustrated in FIG. 3B, may be set to a minimum density, nominal density, or a maximum density achievable in a particular process technology. In some realizations, the process corners for the dielectric constant may also be varied across different instances of capacitive load 108 to isolate the effects of these process parameters on interconnect delay. The achievable parameters, e.g., line widths, metal thickness, line density, and dielectric constant of insulators, typically vary with variations in process technology.

Applicant respectfully maintains that claim 7 satisfies the requirements of 35 U.S.C. § 112. Accordingly, Applicant respectfully requests the objection to claim 7 be withdrawn.

Regarding claim 8, the Office action states that it is not clear what is meant by "maximum density." Applicant respectfully points the Examiner to paragraph [1022] of the specification, which states:

> In addition, the density, i.e., the spacing relationship between a metal trace and adjacent metal traces, as illustrated in FIG. 3B, may be set to a minimum density, nominal density, or a maximum density achievable in a particular process technology. In some realizations, the process corners for the dielectric constant may also be varied across different instances of capacitive load 108 to isolate the effects of these process parameters on interconnect delay. The achievable parameters, e.g., line widths, metal thickness, line density, and dielectric constant of insulators, typically vary with variations in process technology.

Applicant respectfully maintains that claim 8 satisfies the requirements of 35 U.S.C. § 112. Accordingly, Applicant respectfully requests the objection to claim 8 be withdrawn.

Regarding claim 9, the Office action states that it is not clear what is meant by "nominal density." Applicant respectfully points the Examiner to paragraph [1022] of the specification, which states:

> In addition, the density, i.e., the spacing relationship between a metal trace and adjacent metal traces, as illustrated in FIG. 3B, may be set to a minimum density, nominal density, or a maximum density achievable in a particular process technology. In some realizations, the process corners for the dielectric constant may also be varied across different instances of capacitive load 108 to isolate the effects of these process parameters on interconnect delay. The achievable parameters, e.g., line widths, metal thickness, line density, and dielectric constant of insulators, typically vary with variations in process technology.

Applicant respectfully maintains that claim 9 satisfies the requirements of 35 U.S.C. § 112. Accordingly, Applicant respectfully requests the objection to claim 9 be withdrawn.

Claims 13-15 are amended to provide antecedent basis.

Claim Rejections Under 35 USC § 102

Claims 1-15 and 18-19 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U. S. Patent No. 6,463,570 B1 to Dunn et al. (hereinafter, "Dunn"). Regarding claim 1, Applicant respectfully maintains that Dunn, alone or in combination with other references of record, fails to teach or suggest

> a first capacitive load for characterizing at least one layer of an interconnect structure in the integrated circuit, the first capacitive load being selectively coupled to the speed sensing circuit, the first capacitive load being formed by at least a

> portion of a first metal trace residing in a first metal layer and at least a portion of a second metal trace residing in a second metal layer, the first and second metal layers being separated by at least an insulating layer,

as required by claim 1. Dunn teaches ring oscillator circuit 200 formed on an integrated circuit. FIG. 2A. Ring oscillator circuit 200 of Dunn is used to detect localized imperfections in a salicide layer. Col. 3, line 66-col. 4, line 2. Inverter elements 100 and interconnect between inverter elements 100 of ring oscillator circuit 200 of Dunn have associated parasitic resistances and parasitic capacitances. Col. 2, line 64-col. 3, line 12; col. 4, lines 49-56. The output signal of ring oscillator circuit 200 of Dunn is used to determine propagation delays introduced by the parasitic resistances and parasitic capacitances of ring oscillator circuit 200. Col. 4, lines 6-56. The parasitic resistances and parasitic capacitances of Dunn are part of ring oscillator circuit 200. In contrast, claim 1 requires a capacitive load that is selectively coupled to a speed sensing circuit. Nowhere does Dunn teach or suggest a first capacitive load for characterizing at least one layer of an interconnect structure in the integrated circuit, the first capacitive load being selectively coupled to the speed sensing circuit, the first capacitive load being formed by at least a portion of a first metal trace residing in a first metal layer and at least a portion of a second metal trace residing in a second metal layer, the first and second metal layers being separated by at least an insulating layer, as required by claim 1. For at least this reason, Applicant respectfully maintain that claim 1 distinguishes over Dunn and all references of record. Accordingly, Applicants respectfully request that the rejection of claim 1 and all claims dependent thereon, be withdrawn.

Regarding claim 18, Applicant respectfully maintains that Dunn, alone or in combination with other references of record, fails to teach or suggest

> a first capacitive load for characterizing at least one layer of an interconnect structure in the integrated circuit, the first capacitive load being selectively coupled to the speed sensing circuit, the first capacitive load being formed by at least a

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portion of a first metal trace residing in a first
metal layer and at least a portion of a second metal
trace residing in a second metal layer, the first and
second metal layers being nonadjacent metal layers,
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as required by claim 18. Dunn teaches ring oscillator circuit 200 formed on an integrated circuit. FIG. 2A. Ring oscillator circuit 200 of Dunn is used to detect localized imperfections in a salicide layer. Col. 3, line 66-col. 4, line 2. Inverter elements 100 and interconnect between inverter elements 100 of ring oscillator circuit 200 of Dunn have associated parasitic resistances and parasitic capacitances. Col. 2, line 64-col. 3, line 12; col. 4, lines 49-56. The output signal of ring oscillator circuit 200 of Dunn is used to determine propagation delays introduced by the parasitic resistances and parasitic capacitances of ring oscillator circuit 200. Col. 4, lines 6-56. The parasitic resistances and parasitic capacitances of Dunn are part of ring oscillator circuit 200. In contrast, claim 18 requires a capacitive load that is selectively coupled to a speed sensing circuit. Nowhere does Dunn teach or suggest a first capacitive load for characterizing at least one layer of an interconnect structure in the integrated circuit, the first capacitive load being selectively coupled to the speed sensing circuit, the first capacitive load being formed by at least a portion of a first metal trace residing in a first metal layer and at least a portion of a second metal trace residing in a second metal layer, the first and second metal layers being nonadjacent metal layers, as required by claim 18. For at least this reason, Applicant respectfully maintain that claim 18 distinguishes over Dunn and all references of record. Accordingly, Applicants respectfully request that the rejection of claim 18 and all claims dependent thereon, be withdrawn.

Claim Rejections Under 35 USC § 103(a)

Claims 16 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dunn in view of U. S. Patent No. 5,943,488 to Raza. Applicant believes that claims 16 and 17 depend from allowable base claims and are allowable for at least this reason.

Additional Remarks

Claims 1, 2, 18, 19, 28, and 29 are amended to correct grammatical errors.

Claims 40, 41, and 42 are amended to provide antecedent basis.

Claim 30 is amended to clarify language.

Claim 45 is amended to correct a typographical error.

In summary, all claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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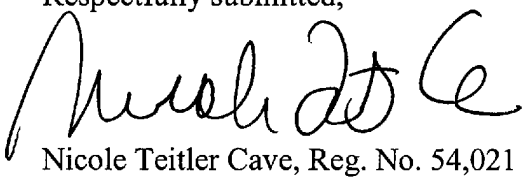

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